MR DOO CONV.
$700.00
PAID

IV. VARIOUS OPTIONAL SETTINGS

A. SERVICE SWITCHES AND DIP SWITCHES

- **Dip Switch A**

1. Number of Mr. Do's (SW1, 2)

No. of Mr. Do's	SW1	SW2
3	OFF	OFF
4	OFF	ON
5	ON	OFF
2	ON	ON

2. Game Style (SW3)

Style	SW3
Table	OFF
Upright	ON

3. Ease or Hardness of "EXTRA" (SW4)

Ease or Hardness	SW4
Easy to win	OFF
Hard to win	ON

4. Ease or Hardness of "SPECIAL" (SW5)

Ease or Hardness	SW5
Easy to win	OFF
Hard to win	ON

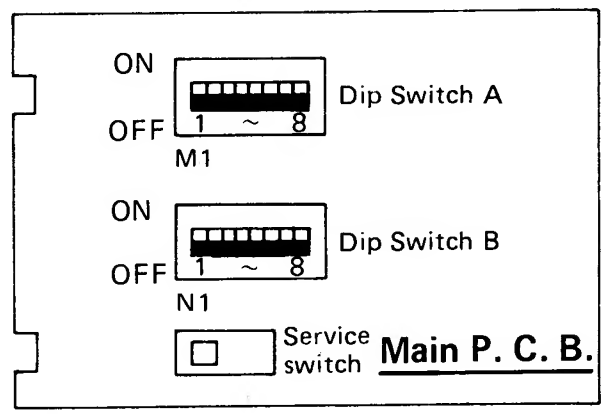
5. Automatic Screen Reneral (SW6)

Automatic screen renewal	SW6
Can	OFF
Cannot	ON

6. Ease or Hardness of Game (SW7, 8)

Ease or Hardness	SW7	SW8
1 (Average)	OFF	OFF
2	OFF	ON
3	ON	OFF
4 (Hard)	ON	ON

- **Position of Dip Switch/Service Switch**



- **Service Switch**

When pressing the service switch, credit is increased by setting the left-side chute.

- **Dip Switch B (Coin & Credit)**

Coin	Credit	Left-side chute				Right-side chute			
		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
1	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
1	2	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
1	3	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
1	4	OFF	OFF	ON	ON	OFF	OFF	ON	ON
1	5	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
2	1	OFF	ON	OFF	ON	OFF	ON	OFF	ON
2	3	OFF	ON	ON	OFF	OFF	ON	ON	OFF
3	1	OFF	ON	ON	ON	OFF	ON	ON	ON
3	2	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
4	1	ON	OFF	OFF	ON	ON	OFF	OFF	ON
1	1	ON	OFF	ON	OFF	ON	OFF	ON	OFF
1	1	ON	OFF	ON	ON	ON	OFF	ON	ON
1	1	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	1	ON	ON	OFF	ON	ON	ON	OFF	ON
1	1	ON	ON	ON	OFF	ON	ON	ON	OFF
Free play		ON	ON	ON	ON	ON	ON	ON	ON

Standard and Custom Price Settings

The game price set by a combination of dip SWs is displayed on the monitor when coin credit is 0.

a) When the settings for right and left chutes are the same, "1 coin — 1 credit", "2 coins — 3 credits", etc. are displayed.

b) When the settings for right and left chutes are provided differently, their respective contents can be displayed.

V.HOW TO CONDUCT SELF-TESTING

★ This machine has a self-testor which locates any abnormalities with the machine should they occur.

[Self-Testing Procedure]

Turn power ON while pressing the push-button or either the 1st or the 2nd player side, and self-testing will follow automatically.

[Self-Testing Items]

(1) ROM Test:
When normal – "ROM OK" will appear on the screen, and the test will proceed to the next step.
When abnormal – "ROM □ □□ " will appear, and the test will be suspended.
□□ Abnormal ROM data
□ Abnormal ROM No.

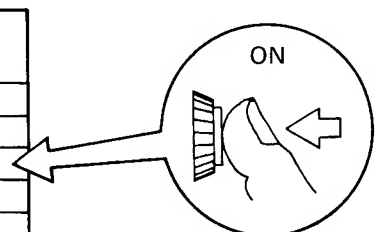
(2) RAM Test:
When normal – "RAM OK" will appear on the screen, and the test will proceed to the next step.
When abnormal – "RAM □ " will appear, and the test will be suspended.
□ Abnormal RAM No.

(3) Sound OFF:
"SOUND OFF" will appear on the screen, and the sound that has been made to that time will stop, then, the test will proceed to the next step. The machine is out of order if the sound does not stop or the test does not proceed to the next step.

(4) Switch Test:
Switch names are displayed on the left side of the screen, while input conditions will be displayed on the right side. When the switch is ON, "0" is displayed for input, and when it is OFF, "1" is displayed. Conduct test while turning each switch ON-OFF – the test will advance to the next step after a minute.

Switch name

TILT		Input condition
SELECT – 2P		1
" – 1P		1
1P side pushbutton		0
1P side joystick	Up	1
"	Right	1
"	Down	1
"	Left	1
COIN	Right	1
	Left	1
Not used		1
2P side pushbutton		1
2P side joystick	Up	1
"	Right	1
"	Down	1
"	Left	1



"0" will appear when pushing the pushbutton on the 1st player's side.

Dip switch A	1	0	1	1	0	1	1	1
" B	1	1	1	1	1	1	1	0

(5) TV Monitor Test:
Cross hatch pattern will appear on the entire screen. Monitor adjustment can be done by means of the pattern.

- Self-testing will stop at this point. Turn ON power again when you want to resume game or execute self-test again.

* In case you have found any abnormality as a result of the self-test, contact the dealer who sold the machine to you.

X. CIRCUIT BOARD

A. CIRCUIT BOARD IC LOCATION AND PARTS LIST

a) Main circuit board IC location and parts list

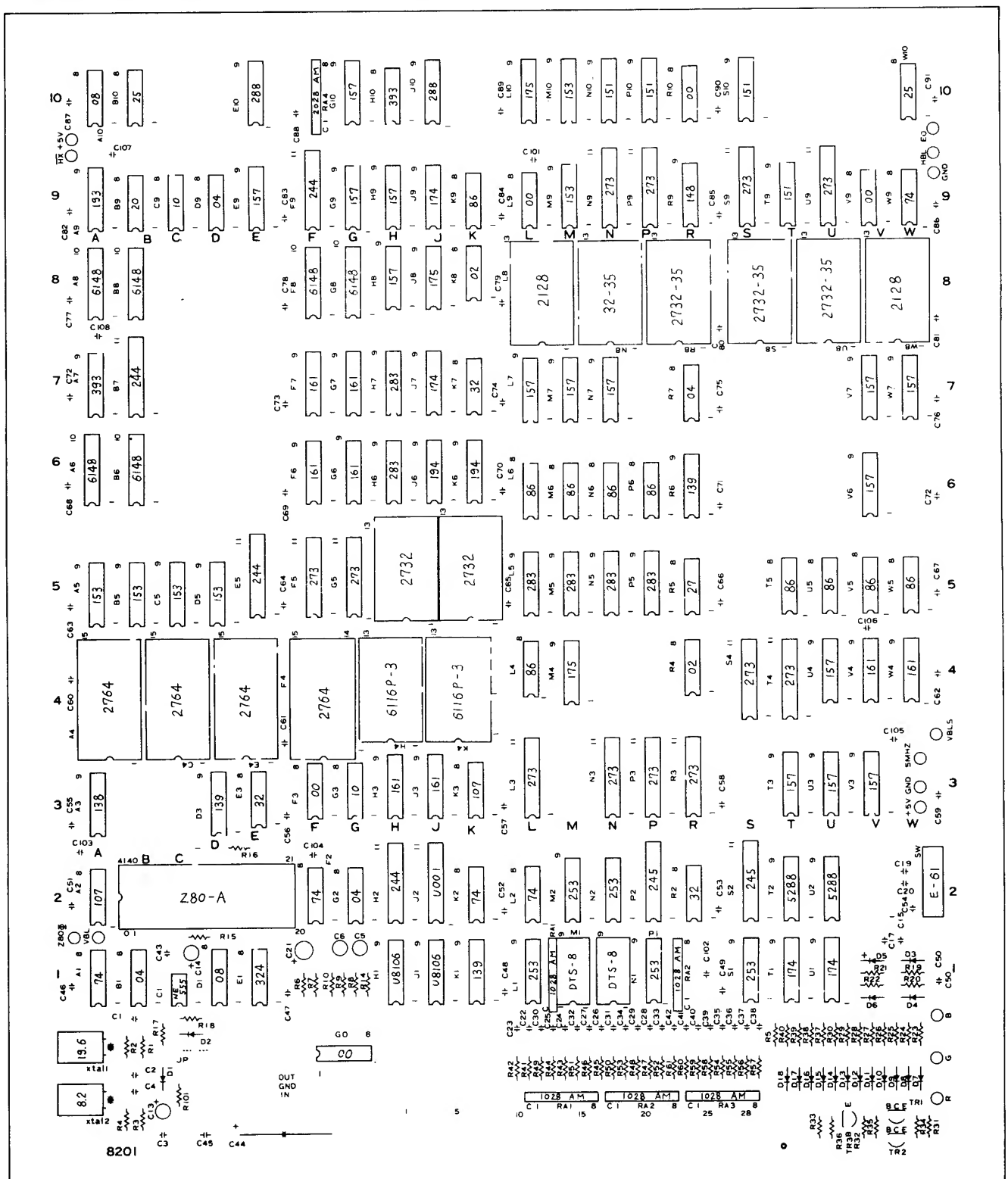


Fig. 18 Main Circuit Board

[1] Integrated Circuit

Item No.	Q'ty	Description
74LS 00	6	TTL
74LS 02	2	"
74LS 04	3	"
74 S 04	1	"
74LS 08	2	"
74LS 10	2	"
74LS 20	1	"
74 25	2	"
74LS 27	1	"
74LS 32	3	"
74LS 74	5	"
74LS 86	10	"
74LS107	2	"
74 148	1	"
74LS151	4	"
74LS153	6	"
74LS138	1	"
74LS139	3	"
74LS157	15	"
74LS161	8	"
74LS174	4	"
74LS175	3	"
74LS193	1	"
74LS194	2	"
74LS224	4	"
74LS245	2	"
74LS253	5	"
74LS273	13	"
74LS283	6	"
74LS393	2	"
74 S288 (TBP18S030)	4	256 bits Fuse ROM
U001	1	Special Function
NE555	1	Timer
Z80A	1	NMOS CPU (4MHz)
2732	6	NMOS 32K bits EP ROM (Access 350nsec)
2764	4	NMOS 64K bits EP ROM (Access 300nsec)
6148P	6	CMOS 4K bits High Speed RAM (Access 70nsec)
6116R-3	2	CMOS 16K bits Static RAM (Access 150nsec)
2128	2	NMOS 16K bits Static RAM (Access 200nsec)
LM324	1	Quad Operational Amplifiers
U8106	2	Programable Sound Generator

[2] Other Semiconductor Devices

Item No.	Q'ty	Description
2SC2785	3	Transistor
10D-1	4	Diode
1S1588	12	"

[3] Capacitors

Rating	Q'ty	Description
50PF/ 12V	2	Ceramic Capacitor
100PF/ "	1	"
220PF/ "	3	"
470PF/ "	1	"
0.01μF/ "	2	"
0.1μF/ "	70	"
10μF/ 16V	2	Chemical Capacitor
47μF/ "	1	"
1μF/ "	2	" (Nonpolar)

[4] Registors

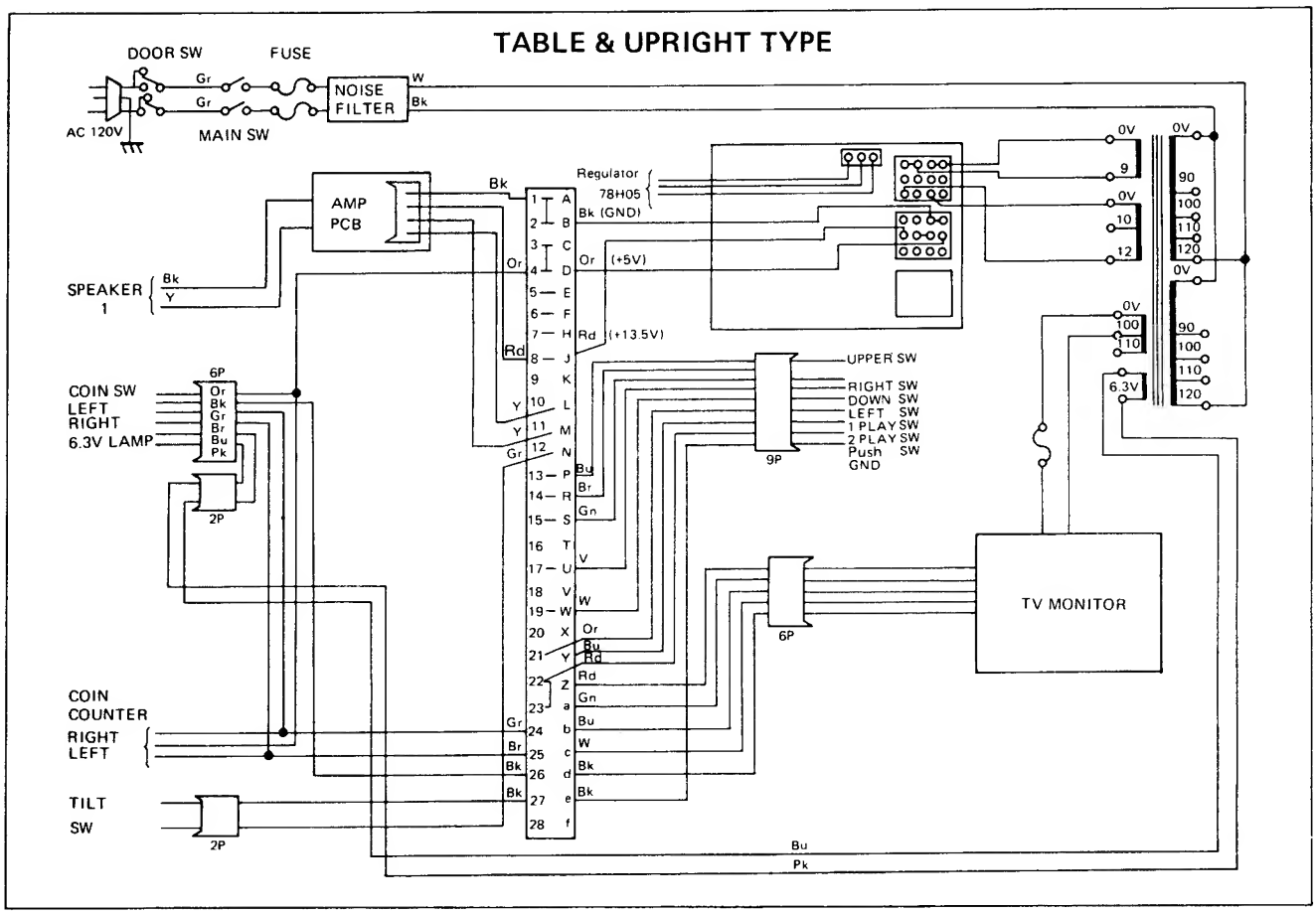
Rating	Q'ty	Description
47Ω ¼W	1	Carbon Solid
51Ω "	3	"
75Ω "	3	"
100Ω "	7	"
120Ω "	3	"
150Ω "	3	"
200Ω "	24	"
220Ω "	3	"
330Ω "	1	"
1KΩ "	1	"
3KΩ "	1	"
10KΩ "	2	"
47KΩ "	2	"
100KΩ "	3	"
MS1028AM	5	1KΩ Registor Array
MS2028AM	1	2KΩ Registor Array

[5] Misc

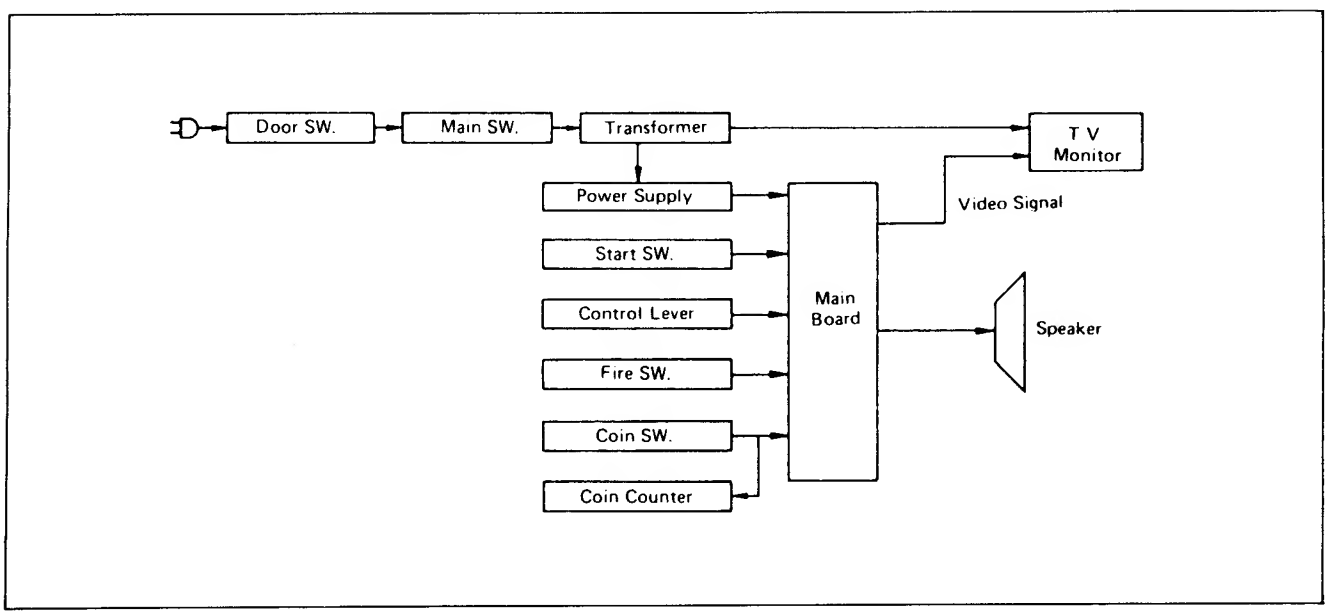
Name	Q'ty	Description
Dip SW	2	8 Elements Switch Array
X tal	2	8.2MHz 19.6MHz
E61-00A	1	Micro SW

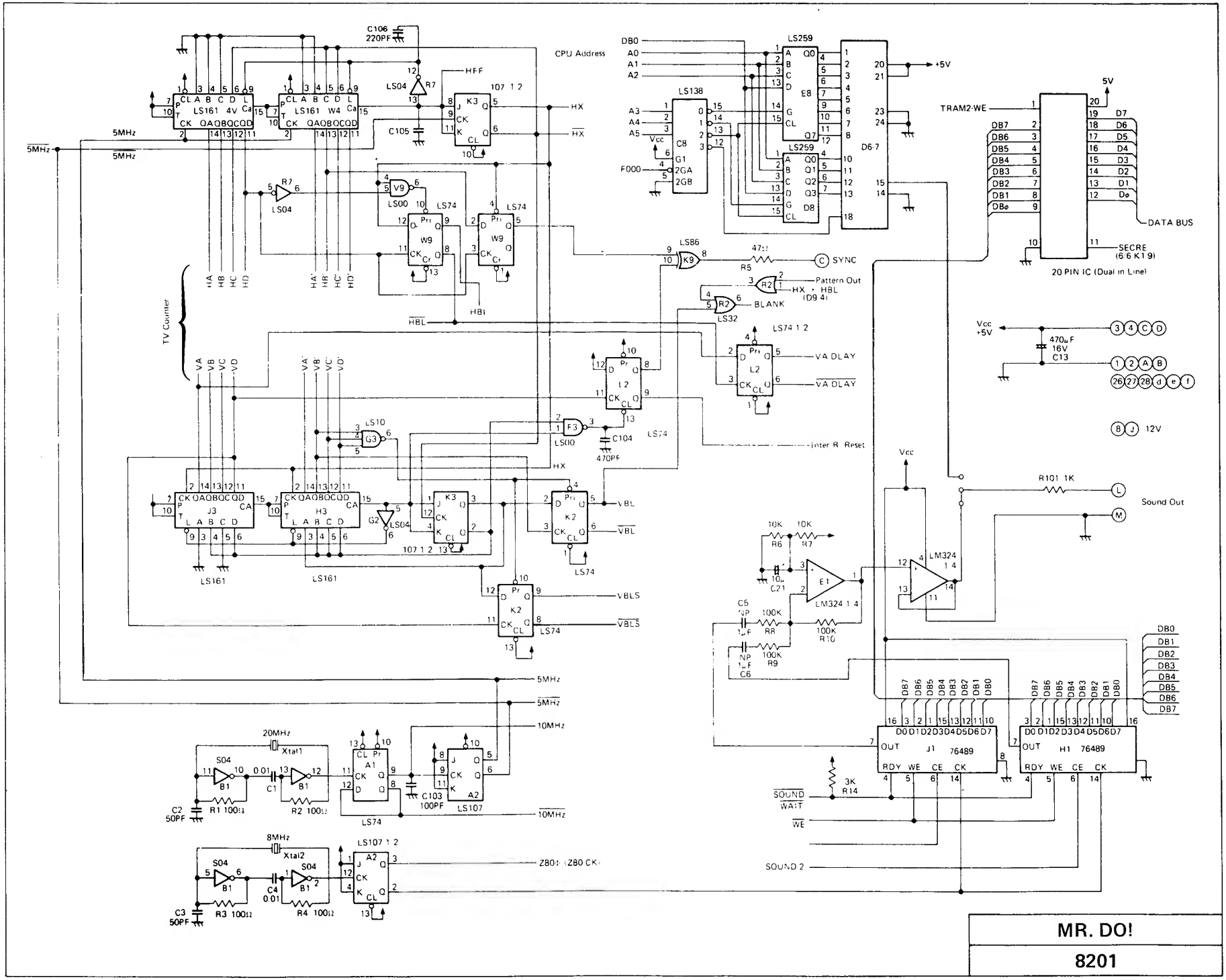
This drawing provides standard information. Universal reserves the right to change without notice.

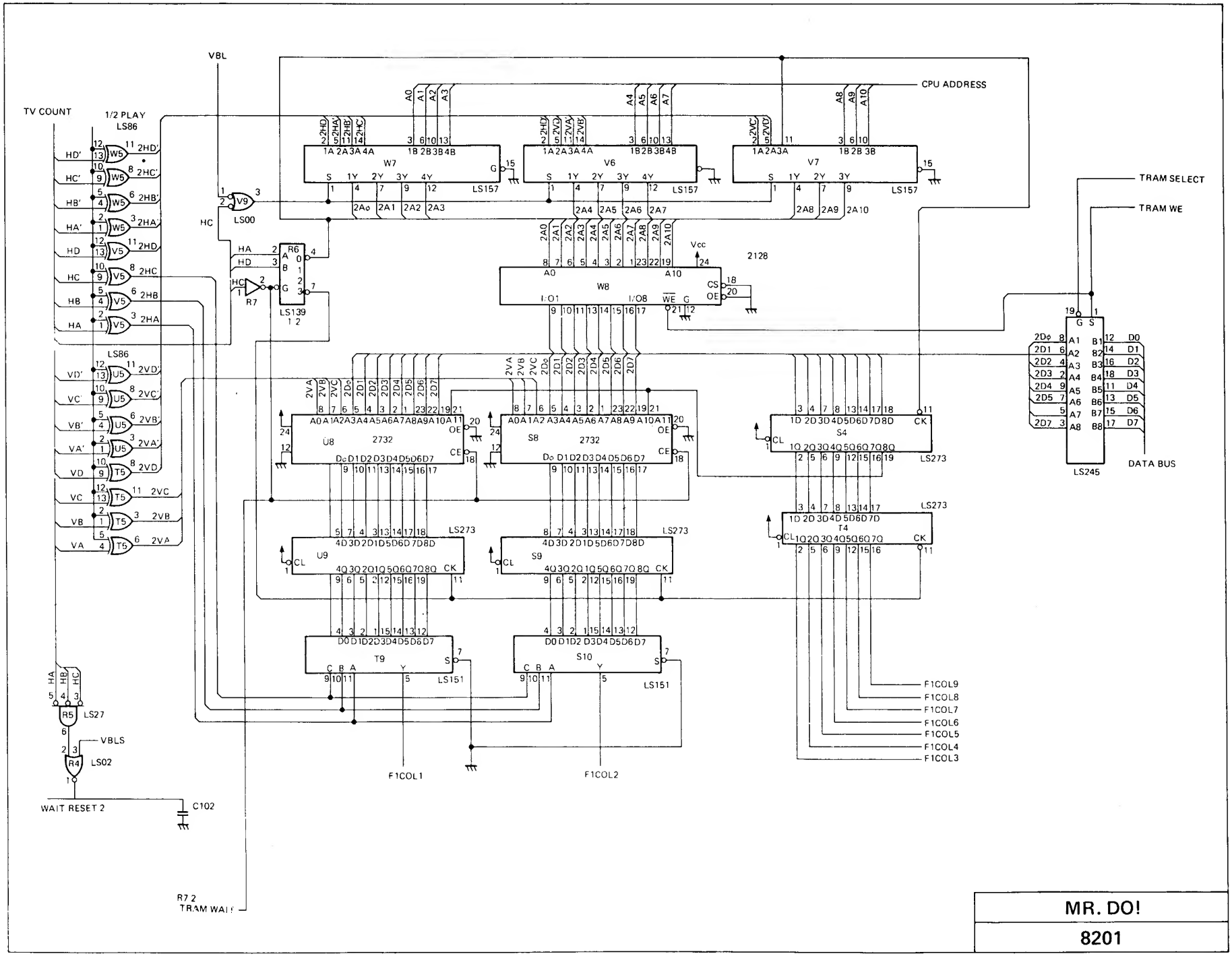
WIRING DIAGRAM (CONNECTOR)



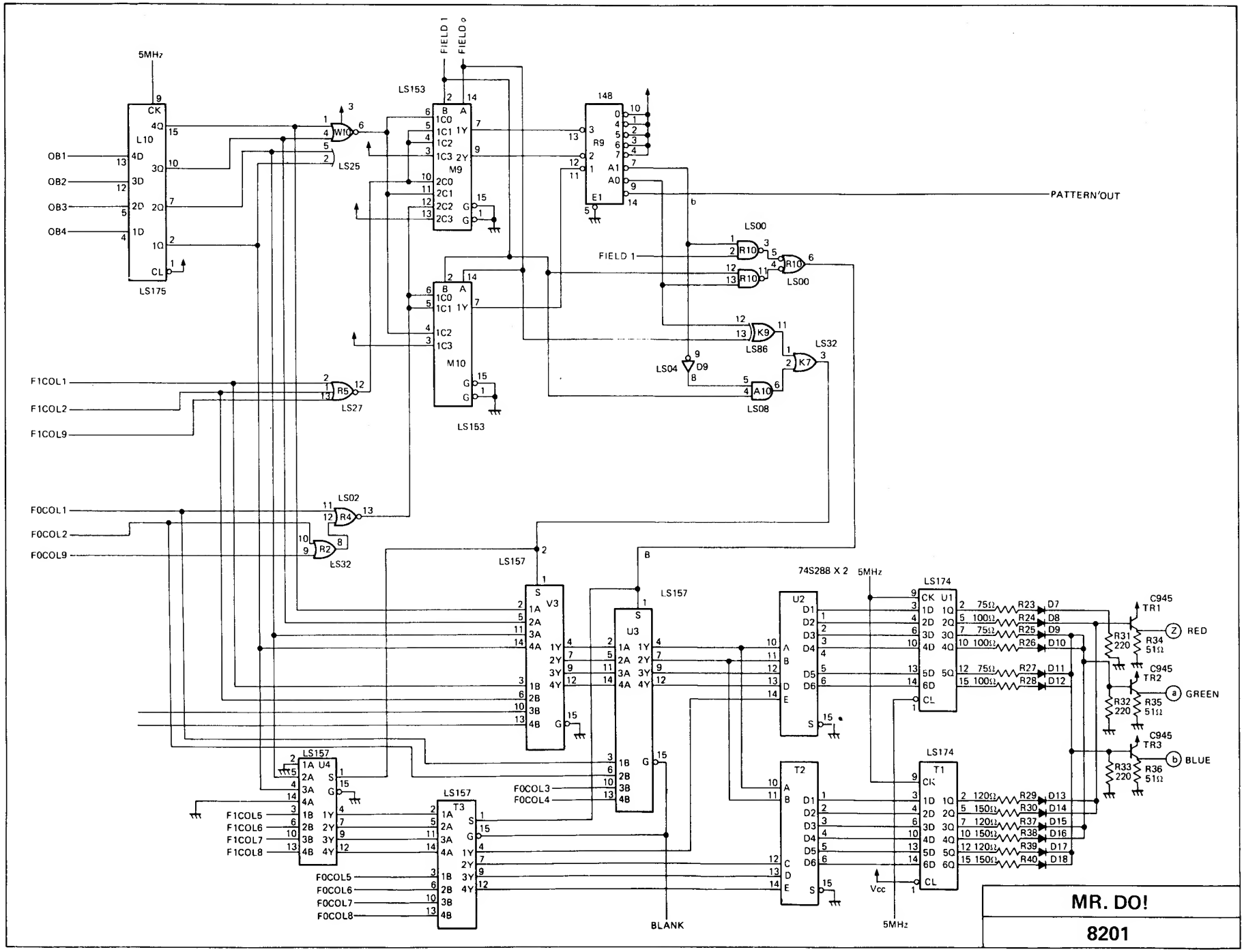
BLOCK DIAGRAM

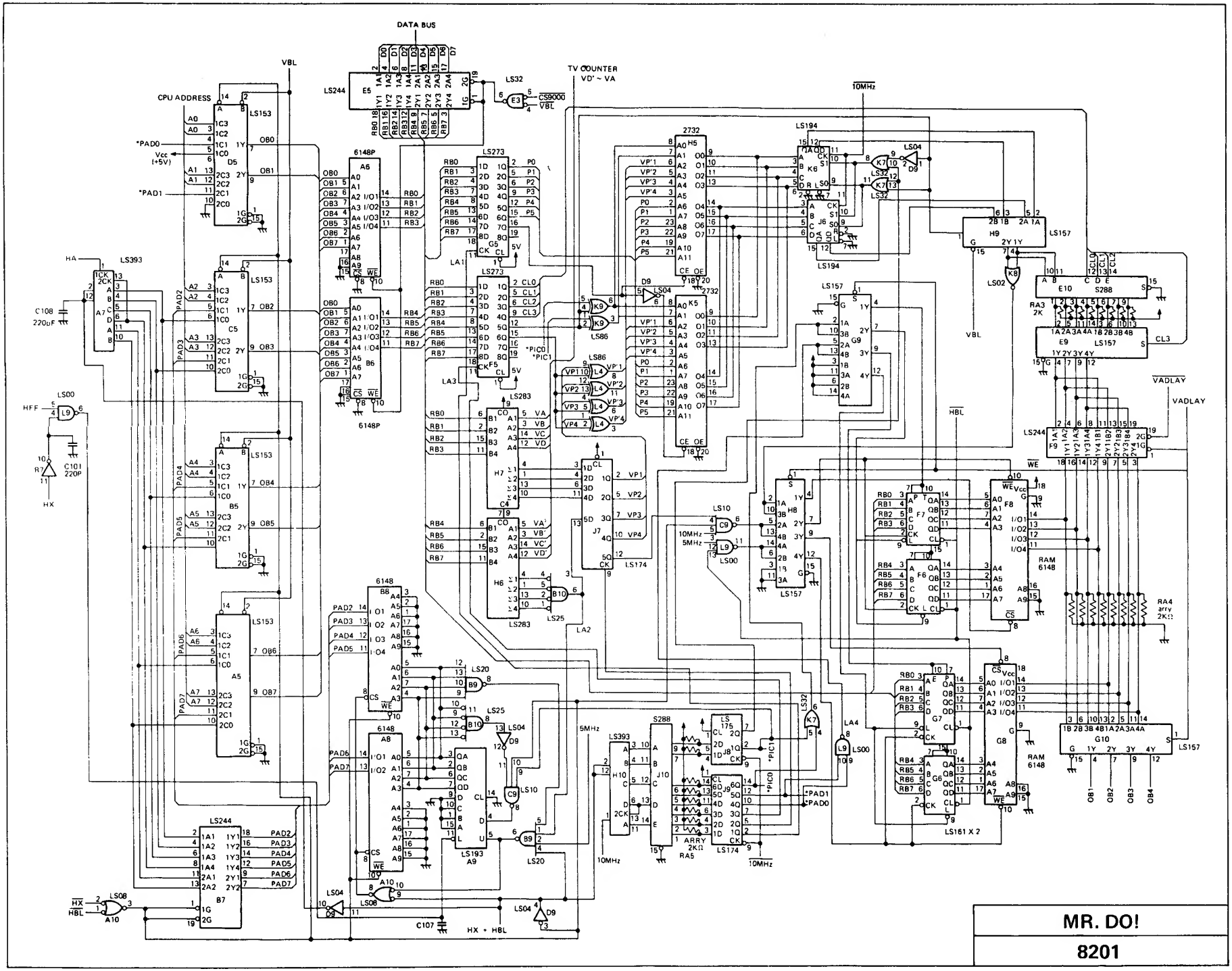



MR. DO!
8201

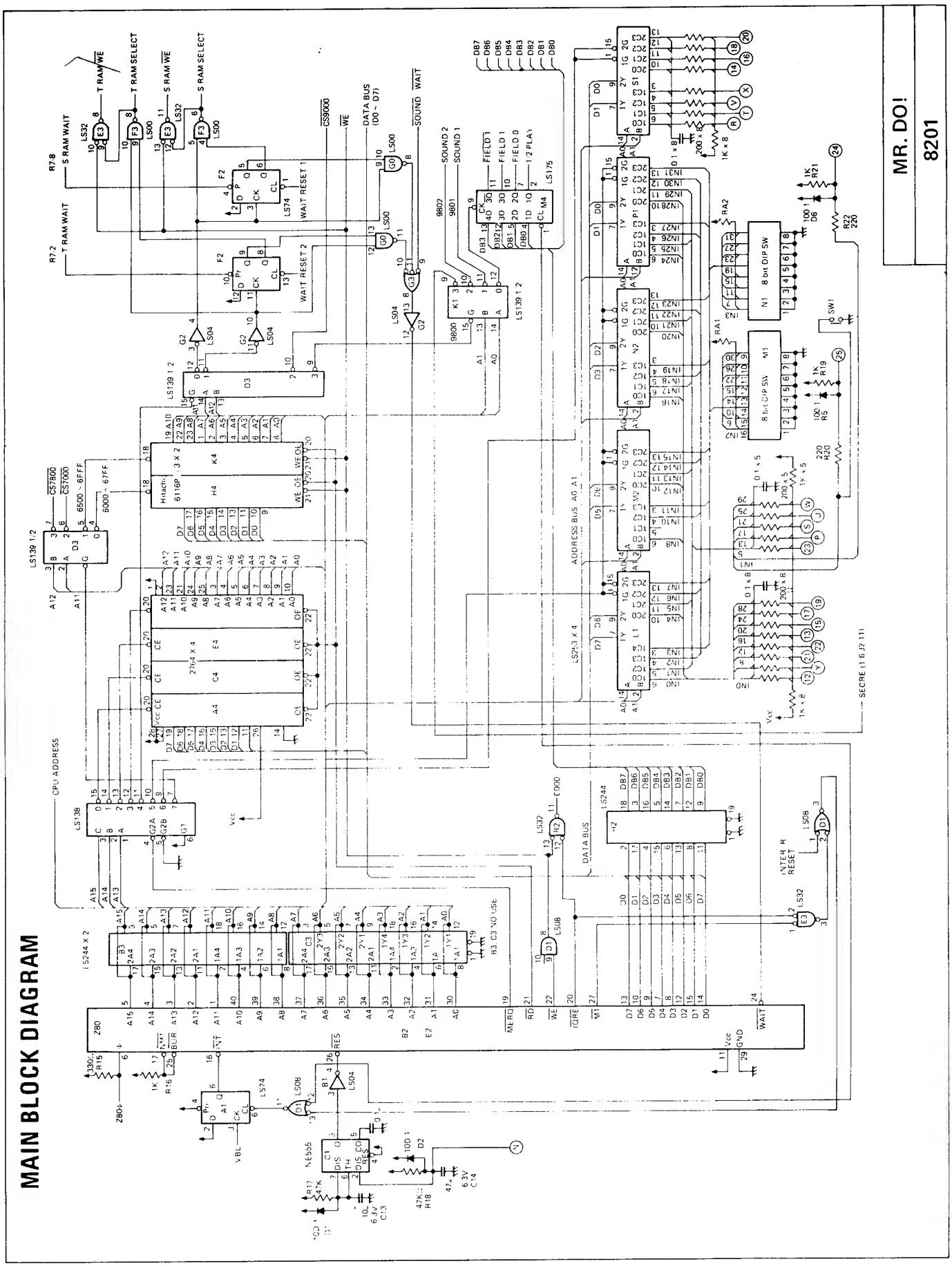

VBL
CPU ADDRESS
TV COUNT
1/2 PLAY
LS86
W7
V6
V7
LS157
TRAM SELECT
TRAM WE
HC
LS00
R6
R7
LS139
2128
W8
Vcc
LS86
U8
2732
S8
S4
LS273
LS245
DATA BUS
U9
S9
T4
T9
S10
LS151
F1COL1
F1COL2
F1COL9
F1COL8
F1COL7
F1COL6
F1COL5
F1COL4
F1COL3
R5
LS27
R4
LS02
VBLS
WAIT RESET 2
C102
R7 2
TRAM WAIT

MR. DO!
8201

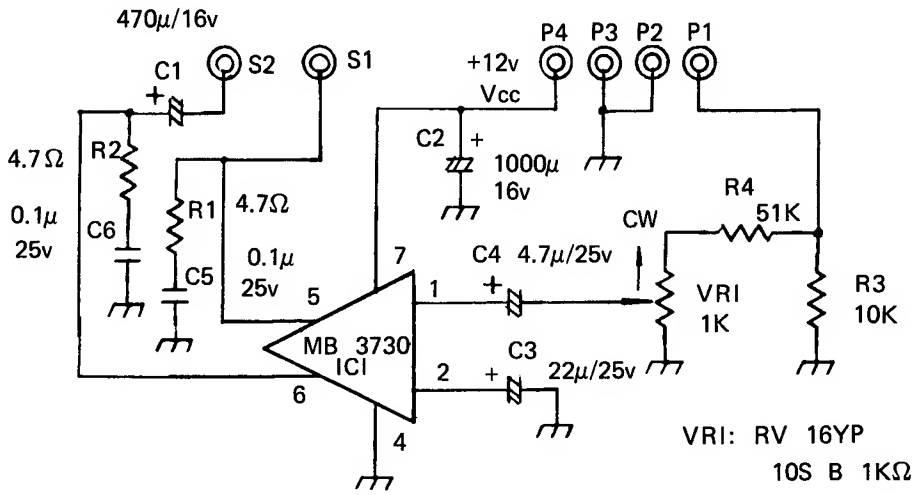

5MHz
FIELD 1
FIELD 0
LS153
L10
LS175
OB1
OB2
OB3
OB4
LS25
M9
M10
148
R9
PATTERN OUT
LS00
FIELD 1
LS86
LS32
LS04
D9
LS08
F1COL1
F1COL2
F1COL9
LS27
F0COL1
F0COL2
F0COL9
LS02
LS157
V3
U3
74S288 X 2
U2
T2
T1
T3
U4
LS174
F1COL5
F1COL6
F1COL7
F1COL8
F0COL5
F0COL6
F0COL7
F0COL8
F0COL3
F0COL4
BLANK
Vcc
C945
TR1
TR2
TR3
RED
GREEN
BLUE
MR. DO!
8201

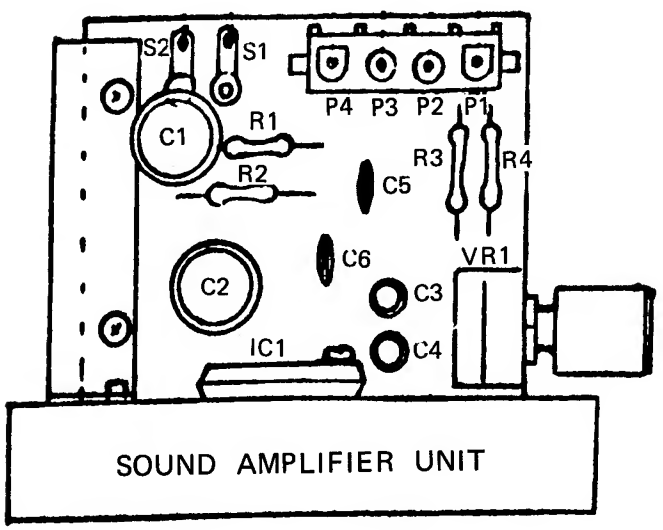

DATA BUS
VBL
CPU ADDRESS
TV COUNTER
VD' ~ VA
10MHz
VADLAY
HX + HBL
MR. DO!
8201

MAIN BLOCK DIAGRAM

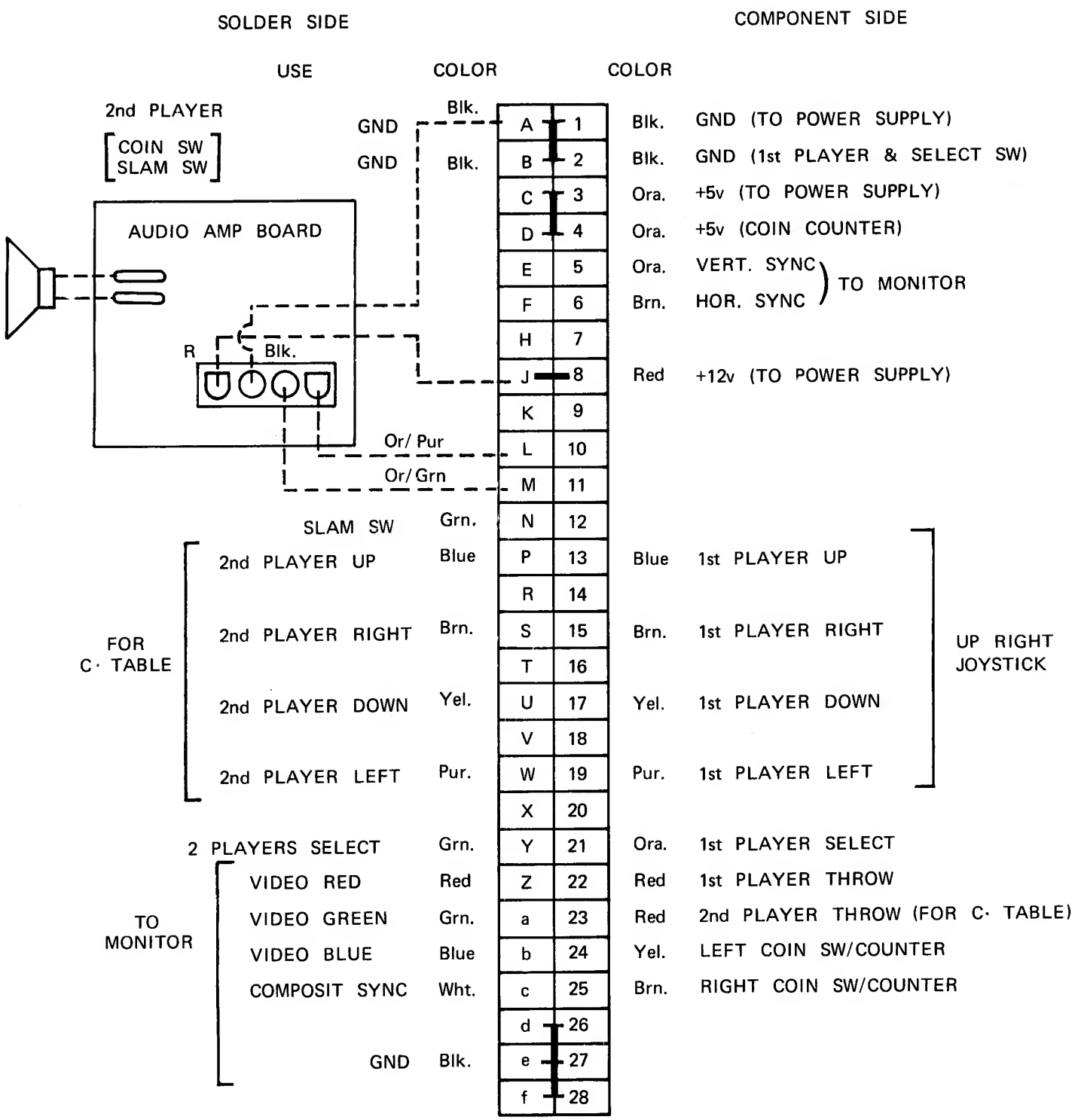


SOUND AMPLIFIER DIAGRAM AND PARTS LOCATION

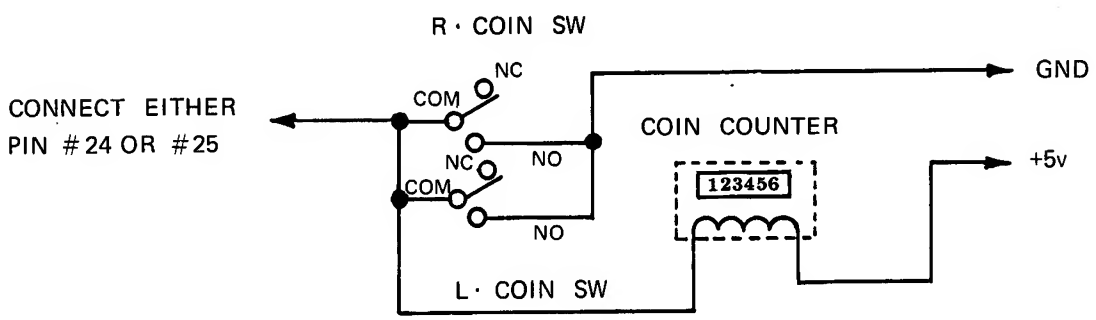




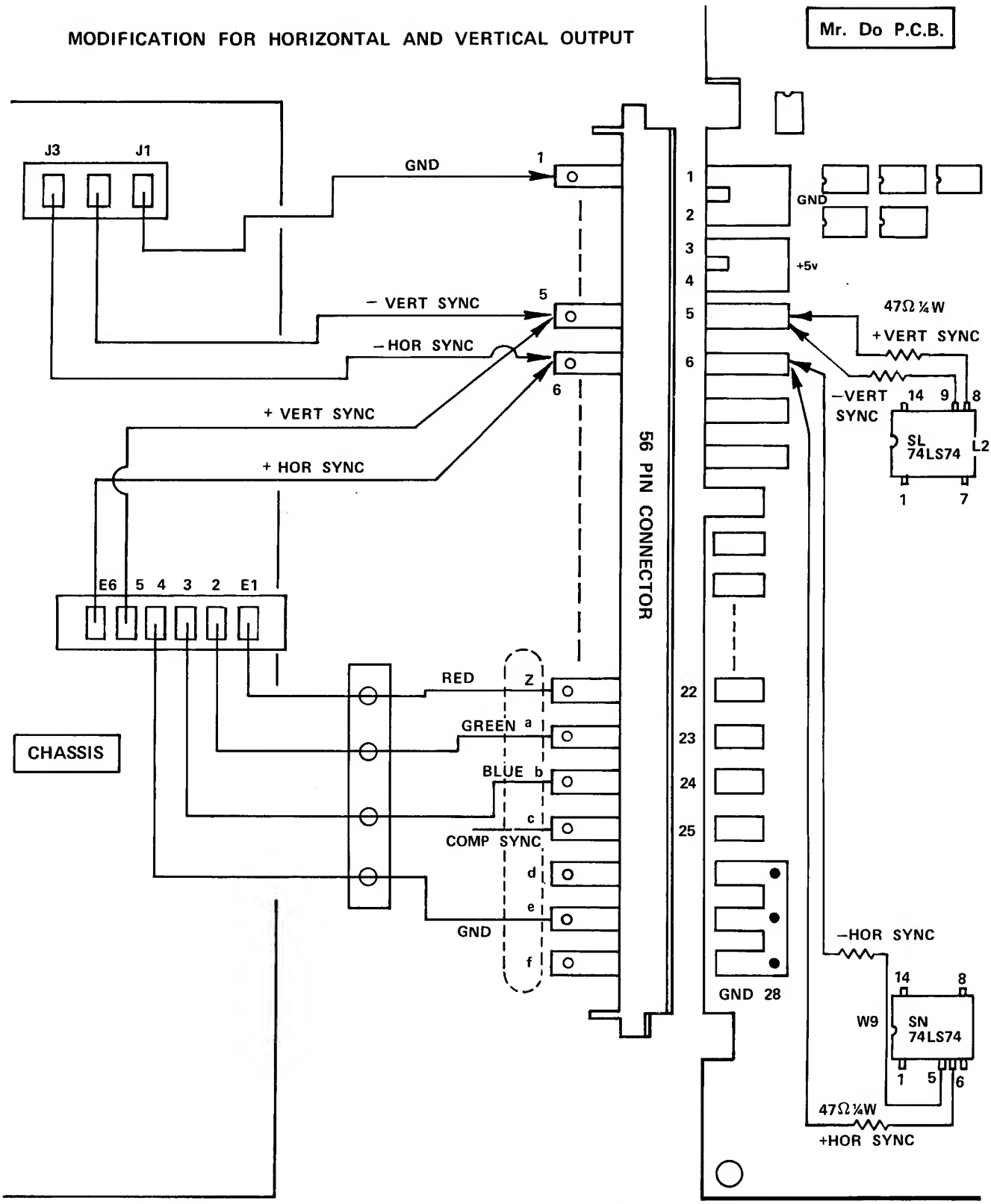
Mr. Do HARNESS PIN ASSIGNMENT



NOTE: CONNECTION FOR USE WITH ONE COIN COUNTER



MODIFICATION FOR HORIZONTAL AND VERTICAL OUTPUT



DEPENDING ON CHASSIS, USE ONE OF THE FOLLOWING MODIFICATIONS:

1. COMP SYNC
2. POSITIVE IND. SYNC
3. NEGATIVE IND. SYNC

BE SURE TO REMOVE COMP SYNC LINE WHEN INSTALLING EITHER THE POSITIVE OR NEGATIVE INDEPENDENT SYNC LINES.